The Data Acquisition System for the KOTO Detector

Stephanie Su University of Michigan

On behalf of

Jia Xu¹, Arjun Sharama², Myron Campbell¹, Monica Tecchio¹, Yasuyuki Sugiyama³, Jon Ameel¹, Celeste Carruth¹, Nikola Whallon¹, Jessica Micallef¹, Tejin Cai², Melissa Hutcheson¹

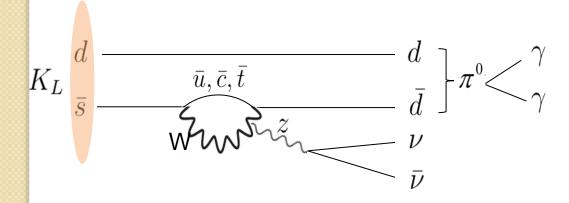
¹University of Michigan

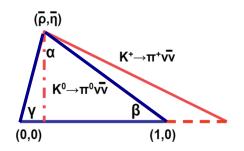
²University of Chicago

³Osaka University

The KOTO Experiment

- Study of rare K_L^0 decay at **To**kai, Japan
 - Measure the branching ratio of $K_L \rightarrow \pi^0 \nu \overline{\nu}$ decay Standard model: $(2.43\pm0.39\pm0.06)\times 10^{-11}$ [J.Brod, et al. PRD 83, 034030 (2011)]
 - Direct CP violating process $\propto \eta^2$
 - Study FCNC and probe for new physics





Previous Results

Direct Limit:

- E39 la at KEK [PRD 81, 072004, 2010] BR($K_1 \rightarrow \pi^0 \nu \overline{\nu}$) < 2.6×10⁻⁸ at 90% CL

Indirect Limit:

- E949 at BNL [PRL 101, 191802, 2008] Measure BR(K⁺ $\rightarrow \pi^+ \nu \bar{\nu}$) = (17.3 \pm 11.0) \times 10⁻¹¹

Grossman-Nir Relation [Y. Grossman and Y. Nir, Phys. Lett. B 398, 163 (1997)] BR($K_L \to \pi^0 \nu \overline{\nu}$) $< 4.4 \times BR(K^+ \to \pi^+ \nu \overline{\nu})$ $\to BR(K_L \to \pi^0 \nu \overline{\nu}) < 1.7 \times 10^{-9} \text{ at } 90\% \text{ CL}$

Goal:

- Standard model: (2.4±0.4)×10⁻¹¹ [J.Brod, et al. PRD 83, 034030 (2011)]

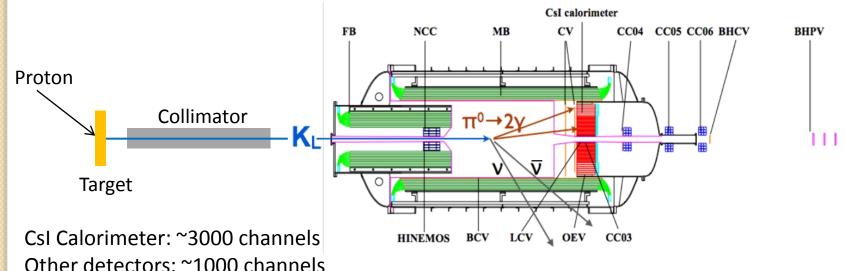
The KOTO Experiment

At J-PARC 30GeV Main Ring May, 2013

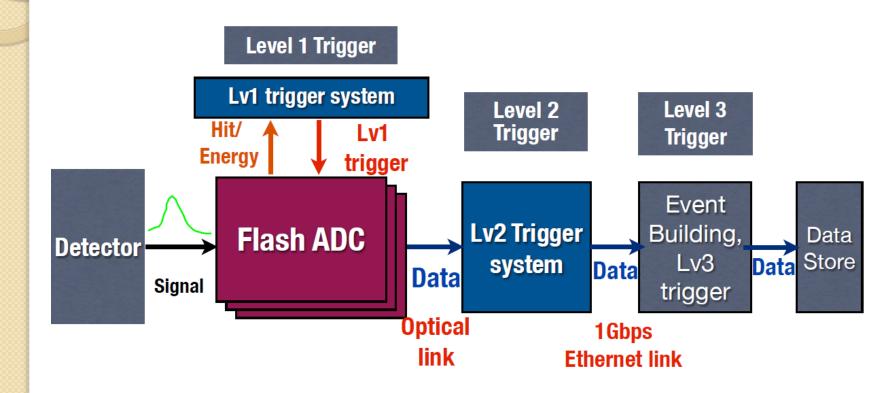
- 24kW proton beam power
- Slow extraction with spill time: 2s/6s
- $3x10^{13}$ POT/spill \rightarrow 6.3x10⁶ K₁/spill

[preliminary, T. Masuda, 2014, Development and Experimental Study of the KOTO Detector System using Three KL Neutral Decay Modes, Kyoto University, Japan]

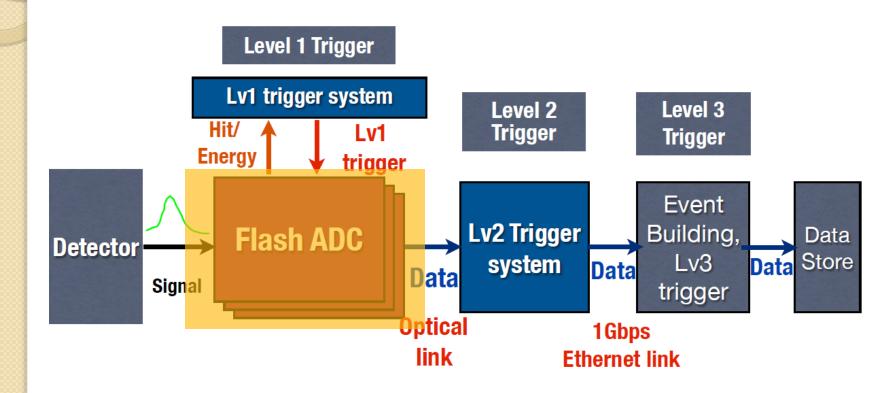




Overview of KOTO DAQ System

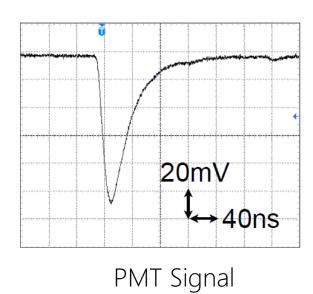


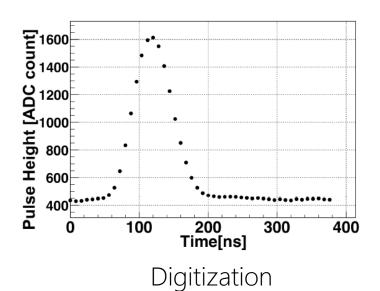
Overview of KOTO DAQ System



ADC

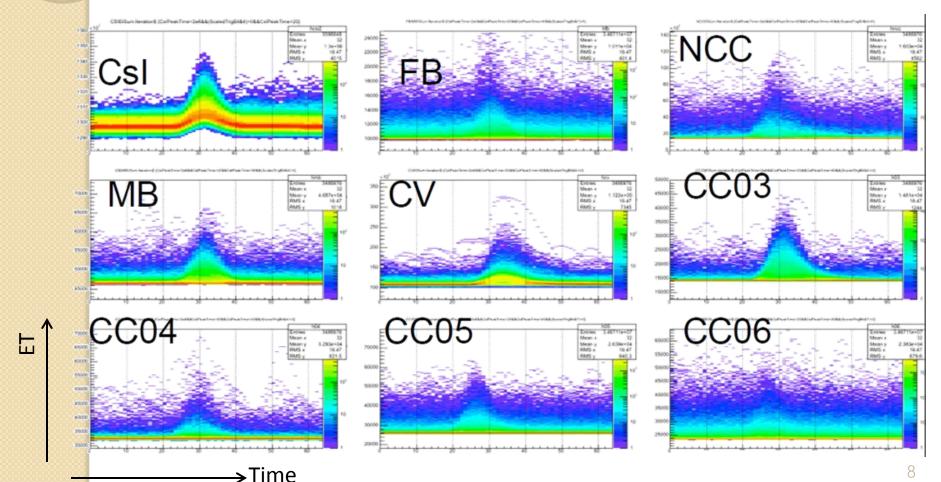
- Each ADC module has 16 channels
- Shape the analog input into Gaussian of 100ns at FWHM
- Digitize the shaped signal with 14-bit at 125MHz

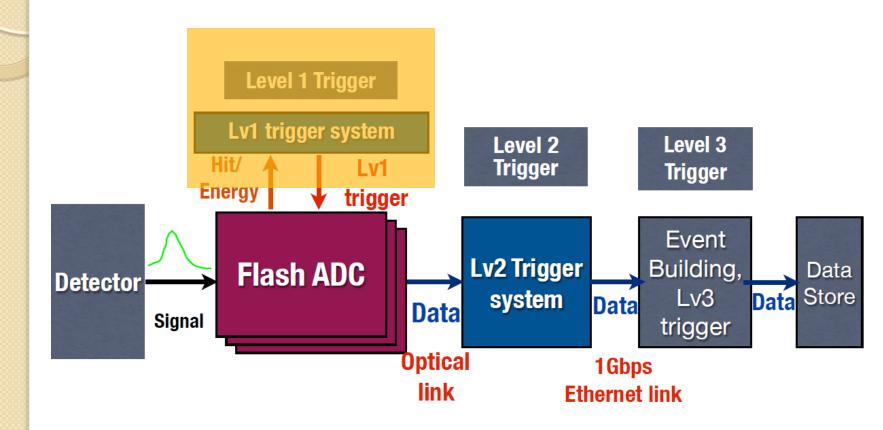




Timing Alignment

 Most of the detectors are aligned with the CSI calorimeter and in the event window (64 clock width)

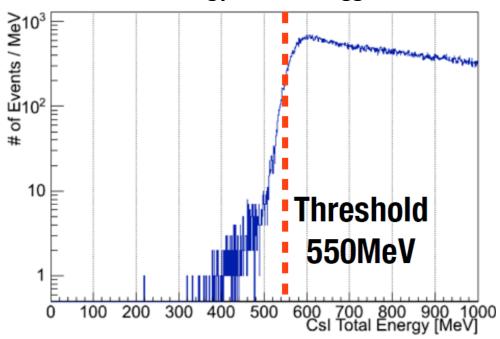




L1 Trigger

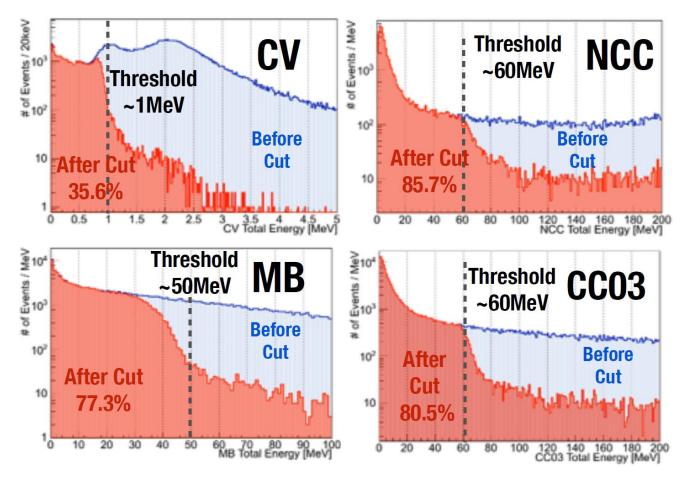
Energy cut on sum of the CsI calorimeter energy

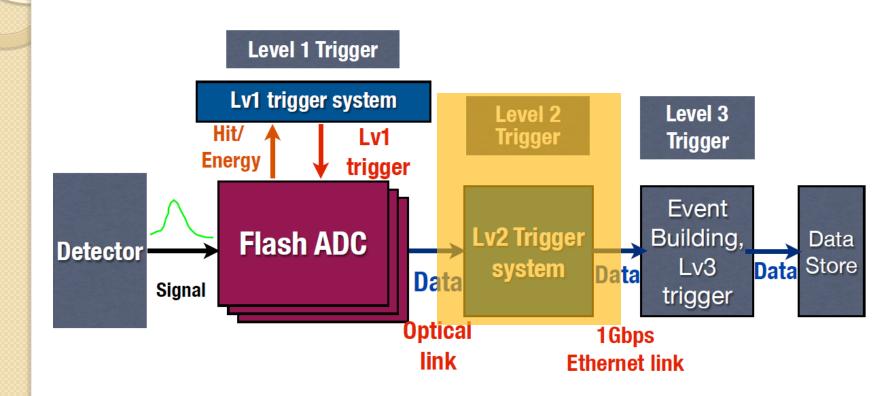
Csl Total Energy after L1 Trigger Events



L1 Trigger

- Energy cut on sum of the CsI calorimeter energy
- Low energy cut for veto detectors

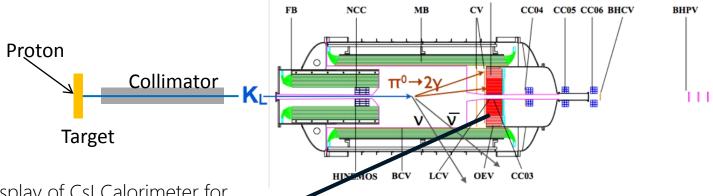




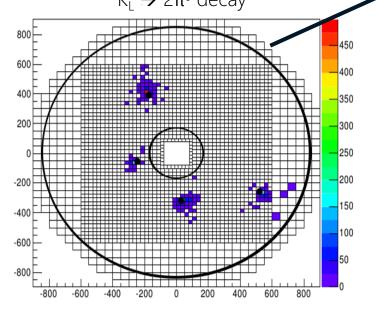
L2 Trigger

- Perform Center Of Energy (COE) radius cut
- $COE = \frac{\sqrt{(\sum_{i} E_{i} x_{i})^{2} + (\sum_{i} E_{i} y_{i})^{2}}}{\sum_{i} E_{i}}$

- $K_L \rightarrow \pi^0 \nu \overline{\nu}$ has large COE radius

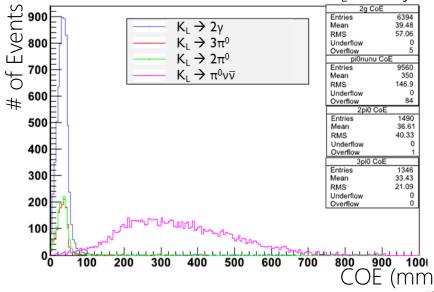


Event Display of Csl Calorimeter for $K_1 \rightarrow 2\pi^0$ decay

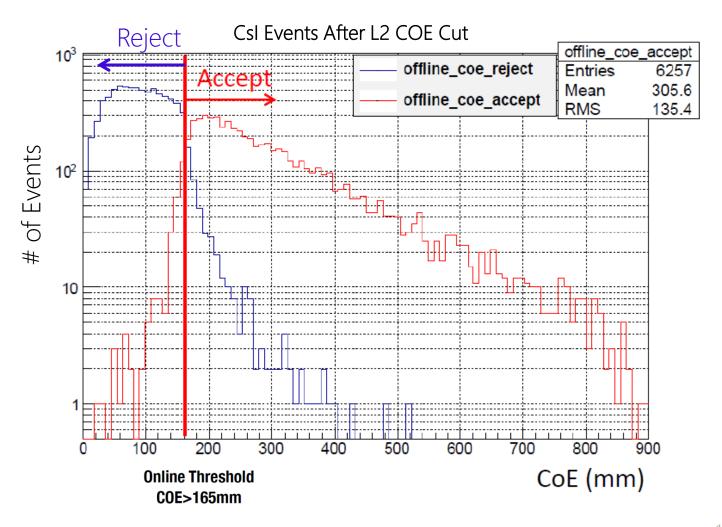


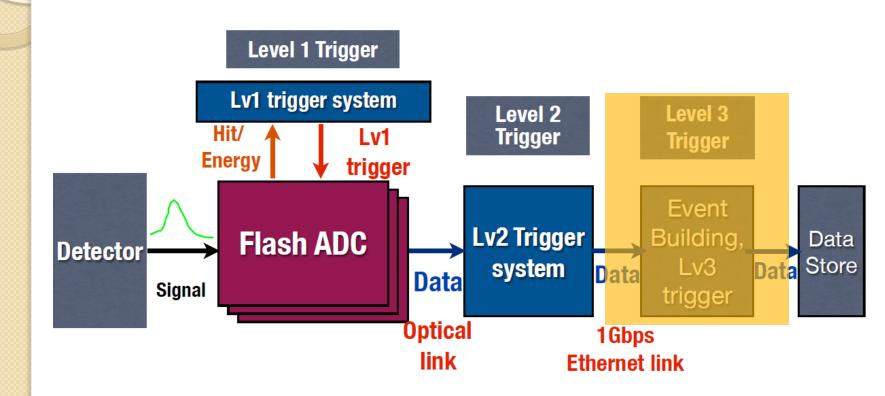
COE Distribution of Different K_L Decays

CsI calorimeter



L2 COE Cut

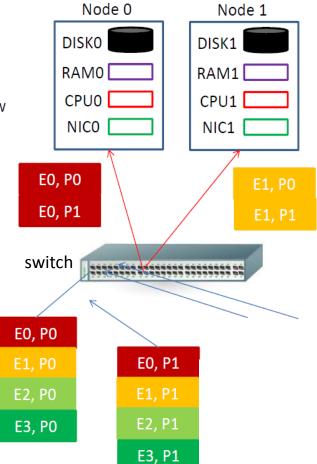




L3 Trigger

System structure

Stream flow

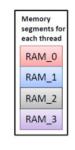


- Computer clusters
- Backend switch do the routing of fragments of single events to the nodes
- Parallel processing using multi-thread
 - 4-thread scheme

L3 Trigger

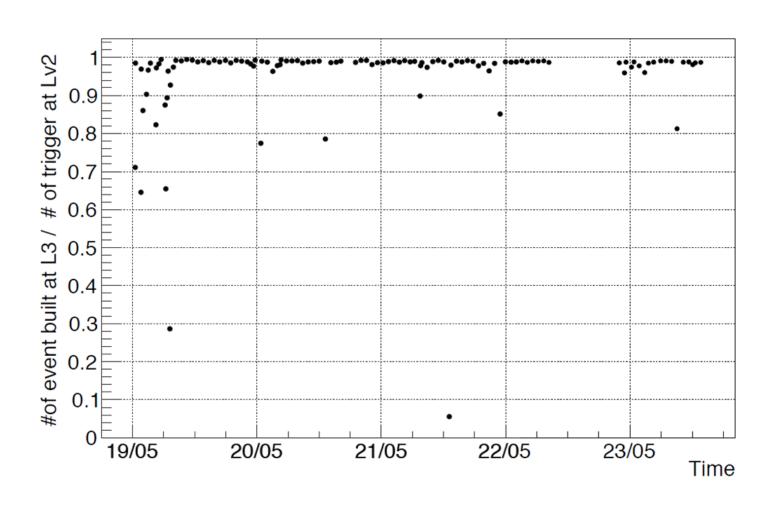
Multi-thread structure

Threads	What thread does	Physical memory operation
Capture thread	Capture events from Ethernet card	NIC → RAM_0
Cut thread	Throw away uninterested events	RAM_0 → RAM_1
Compression on thread	Compression	RAM_1 → RAM_2
Store thread	Copy events into run file in the hard disk	RAM_2 → hard disk



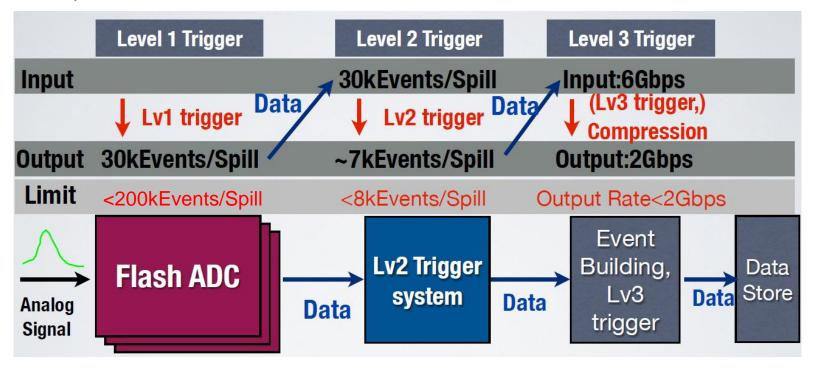
		Capture Thread	Cut Thread	Compression Thread	Store Thread
	Spill 0	RAM_0	IDLE	IDLE	IDLE
time	Spill 1	RAM_1	RAM_0	IDLE	IDLE
10	Spill 2	RAM_2	RAM_1	RAM_0	IDLE
\ [Spill 3	RAM_3	RAM_2	RAM_1	RAM_0
	Spill 4	RAM_0	RAM_3	RAM_2	RAM_1
	Spill 5	RAM_1	RAM_0	RAM_3	RAM_2

L3 Trigger



Data Transfer Rates

- May, 2013
- Spill: 2s/6s

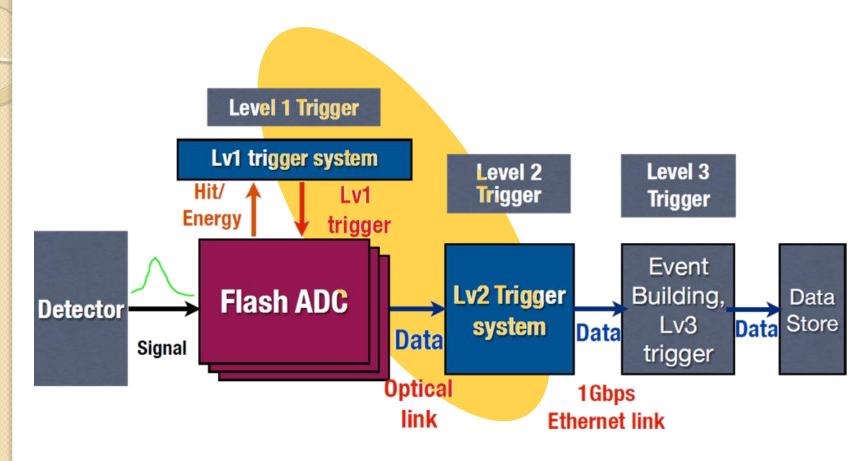


Standard model

 (2.4 ± 0.4) x 10^{-11}

[J.Brod, et al. PRD 83, 034030 (2011)]

L1, L2 DAQ Simulation

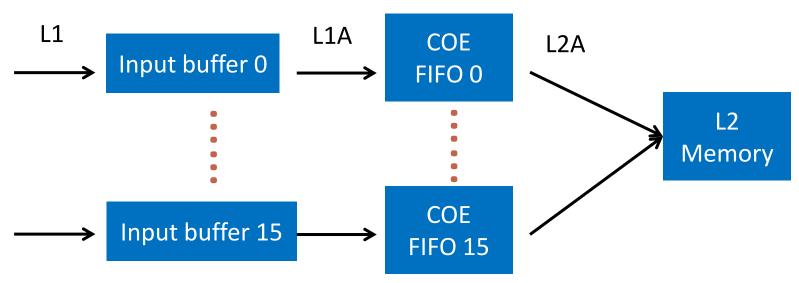


L1 -> L2 DAQ Simulation

L2 Trigger Model

- L1 event from ADC enters input buffer and is accepted (L1A) if buffer is not full
- L1A event wait in COE FIFO for L2 decision
- L2A event is moved from 16 COE FIFOs into single memory
- L2 processing time for uncompressed event (~250kb) is 18000 clock cycles

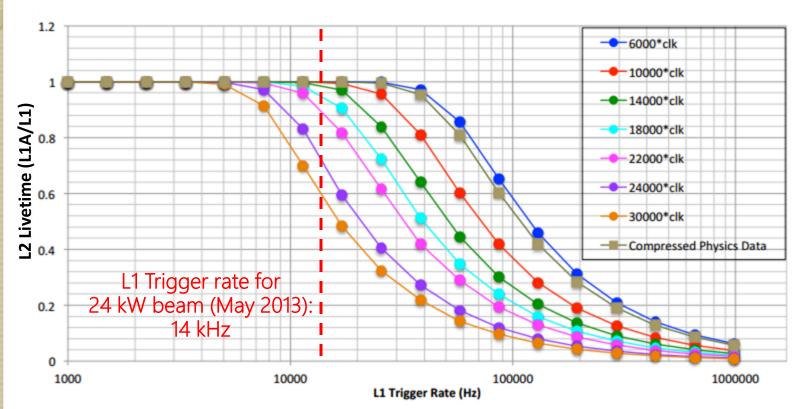
Simulation studies L2 livetime dependence on input buffer size, COE acceptance rate and L2 processing time as a function of L1 trigger rate.



L1 -> L2 Simulation Result

L2 Processing Time

For L2A = 33% and input buffer size = 7 events



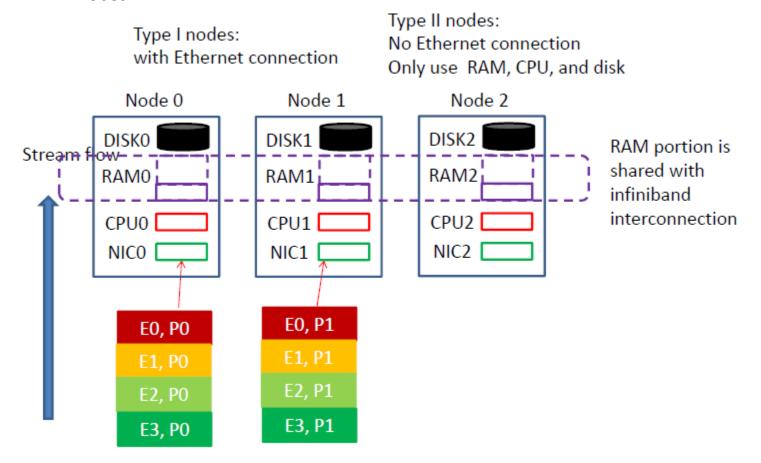
May 2013 DAQ implementation: Cyan points

Compressed data: Brown squares

KOTO DAQ Upgrade

New L3 Architecture

- Event Building: Ethernet → Infiniband
 - Remote direct memory access
 - TCP based connection
 - Uses API



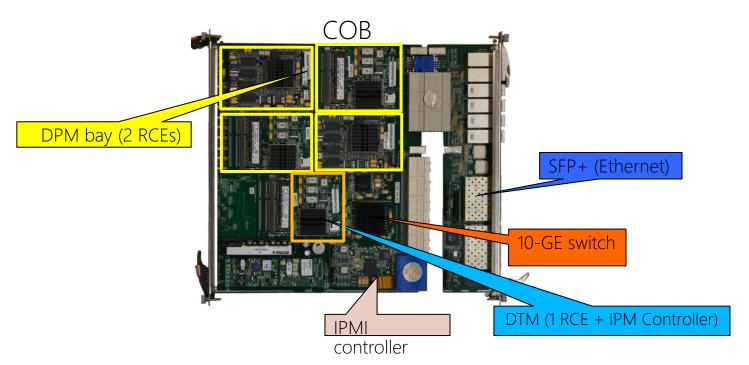
New L3 Architecture

Both Type I and Type II nodes can have the same multi-thread structure.

Threads	What thread does	Physical memory operation
Capture thread	Capture events from Ethernet card	NIC → RAM_x
Switching thread	Target data segments to designated nodes	RAM_x → Whoever's RAM_0 it should go to
Cut thread	Throw away uninterested events	RAM_0 → RAM_1
Compression on thread	Compression	$RAM_1 \rightarrow RAM_2$
Store thread	Copy events into run file in the hard disk	RAM_2 → hard disk

L2 Trigger Upgrade

- Advanced Telecommunication Computing Architecture (ATCA)
 - Allow backend communication (each board can talk to each other)
- Reconfigurable Cluster Element (RCE)
 - Dense and fast connection across different parts of the system (R&D undergoing at SLAC)
- Cluster-On-Board (COB)
 - Dense and fast connection across different parts of the system (R&D undergoing at SLAC)



Conclusion

Current DAQ: Functioned well at 24kW in May, 2013

Short-term upgrade (up to 100kW):

- Online compression to increase L2 Livetime
- New L3 architecture with Infiniband

Long-term upgrade (up to 300kW):

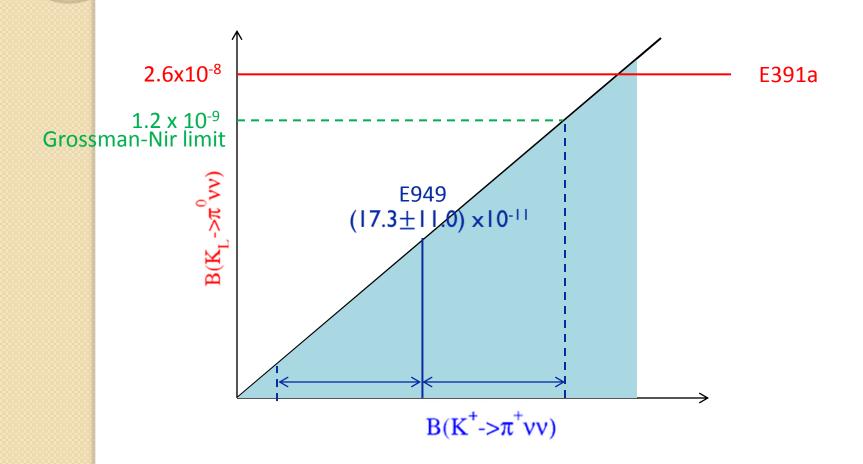
Use L2 trigger with RCE

Backup Slides

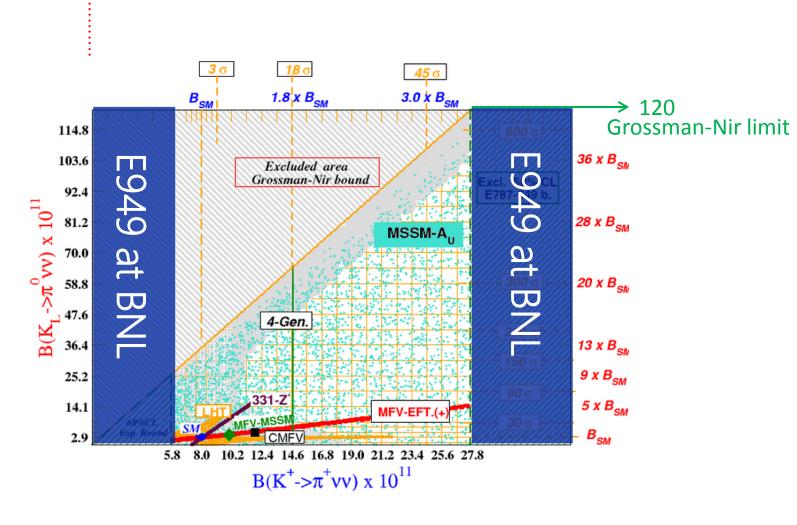
Grossman-Nir Limit

• $BR(K_L \to \pi^0 \nu \overline{\nu}) < 4.4 \times BR(K^+ \to \pi^+ \nu \overline{\nu})$

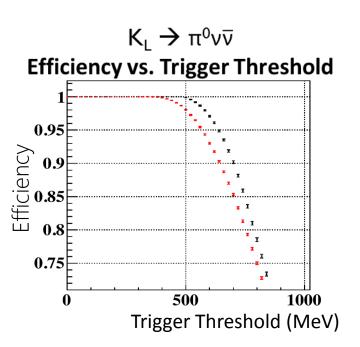
[Y. Grossman and Y. Nir, Phys. Lett. B 398, 163 (1997)]



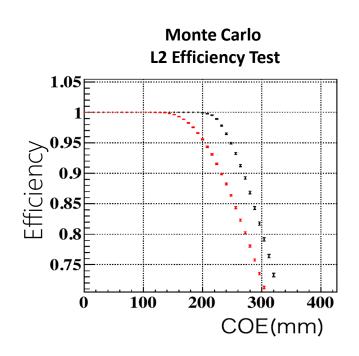




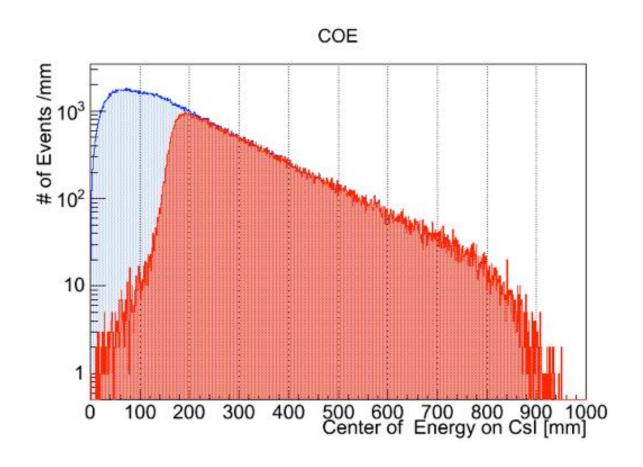
Trigger Efficiency - Monte Carlo



Black: All K_L events after reconstructions Red: K_L events in our signal region



L2 COE Cut



L1 -> L2 DAQ Simulation

- Simulate 2 second spill with rates between 1kHz and 1MHz
 - In 24 kW physics run (Apr. 2013), the L1Req was 14kHz
- Make a decision for L1Req every clock cycle (8ns)
- Each L1Req dumps one packet into the buffer
 - Current DAQ can hold max of 7 packets
 - L1Req is not accepted (L1A) if the input buffer is full
- L2A: 17000 clock cycles
 - Models the time it takes to move 64-sampling uncompressed trigger from 16 fibers (256 ADC)
- L2R: instant

